Listing of the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A programmable interface comprising:

a register file having a plurality of registers, each register having a type;

a run control register;

a microcontroller configured to bidirectionally communicate with the register file and the run control register;

a Code Store SRAM configured to bidirectionally communicate with the microcontroller; and

executable code including one or more instructions;

wherein the Code Store SRAM and the run control register are configured to bidirectionally communicate with a system processor that is external to the programmable interface; and

wherein the system processor is configured to load the executable code onto the Code Store SRAM and is further configured to signal the microcontroller, via the run control register, to begin execution of the one or more instructions included in the executable code; and

wherein the plurality of registers includes (i) a general-purpose microcontroller register, (ii) a timer register, (iii) an external input/output (I/O) interface register, (iv) an internal I/O register, (v) a shared register, (vi) an interrupt register, and (vii) a first-in, first-out (FIFO) register configured to communicate with a direct memory access (DMA) controller.

2. (Cancelled)

3. (Currently Amended) A programmable interface, as defined in claim [[2]] 1, wherein the ~~one of the registers has a type of~~ external I/O interface, ~~the~~ register includes an ~~including~~ edge detect logic.

4. (Cancelled)

5. (Currently Amended) A programmable interface, as defined in claim [[3]] 1, wherein the executable code implements a laser printer mechanism communications interface and a vertical top-of-page synchronization interface.

6. (Previously Presented) A programmable interface, as defined in claim 1, wherein the executable code is selected from a group that includes serial interfaces, parallel interfaces, serial peripheral interface (SPI), Synchronous Serial Interface (SSI), MicroWire, Inter Integrated Circuit (I2C), control area network (CAN), UART, IEEE1284, LCD interface, front panel interface, and MODEM.

7. (Previously Presented) A programmable interface, as defined in claim 1, wherein the system processor is configured to bidirectionally communicate with the register file.

8. (New) A programmable interface, as defined in claim 1, wherein the timer register is configured to (i) increment independently based on a selected system timebase, (ii) generate timing for protocols to be implemented, and (iii) detect protocol timeout errors.

9. (New) A programmable interface, as defined in claim 1, wherein the shared register is accessed by both the system processor and the microcontroller, and wherein the shared register is configured to emulate a peripheral status, wherein an access priority grants write access to either the system processor or the microcontroller for accessing the to the shared register.

10. (New) A programmable interface, as defined in claim 1, wherein the external I/O interface register is configured to (i) facilitate the microcontroller to observe and control actual external electrical signals associated with a protocol of communications of the programmable interface, and (ii) facilitate implementation of a control state machine in the microcontroller.

11. (New) A programmable interface, as defined in claim 1, wherein the internal I/O register is configured to (i) facilitate an I/O subsystem to communicate with internal dedicated function blocks of the programmable interface.

12. (New) A programmable interface, as defined in claim 1, wherein the interrupt register is configured to (i) facilitate an I/O subsystem to provide interrupt-driven status to the system processor.